Please amend claim 1 as follows:

1. (Currently Amended) A system comprising:

a first group of integrated circuits connected in a truncated ring fashion, wherein the truncated ring includes a truncated region to allow for additional integrated circuits to be added to the ring, wherein when the truncated ring is open, one of the integrated circuits immediately next to the truncated region can communicate only in the direction opposite the truncated region and wherein when the truncated ring is closed, the integrated circuit immediately next to the truncated region can also communicate in the direction toward the truncated region.

2. (Original) The system of claim 1, wherein the truncated ring uses point-to-point signaling.

3. (Original) The system of claim 1, wherein the truncated ring is a multidimensional ring.

4. (Original) The system of claim 1, wherein at least one of the integrated circuits that is not a master controller includes a termination resistor in its die.

5. (Original) The system of claim 1, wherein at least one of the integrated circuits that is not a master controller includes a termination resistor in packaging of its die.

6. (Original) The system of claim 1, wherein at least two of the integrated circuits include a termination resistor in its die.

7. (Original) The system of claim 1, wherein at least one of the integrated circuits includes a termination resistor in packaging of its die.

8. (Original) The system of claim 1, wherein one of the integrated circuits acts as a master controller for the other integrated circuits.

9. (Original) The system of claim 1, wherein the integrated circuits use differential signaling.

10. (Original) The system of claim 1, wherein the integrated circuits use pseudo differential signaling.

11. (Original) A system comprising:

a group of integrated circuits connected in a pseudo ring fashion, wherein the pseudo ring is created by data flow of bi-directional signaling between the integrated circuits.

12. (Original) The system of claim 11, wherein the pseudo ring is a multidimensional

ring.

13. (Original) The system of claim 11, wherein at least one of the integrated circuits that is not a master controller includes a termination resistor in its die.

14. (Original) The system of claim 11, wherein at least one of the integrated circuits that is not a master controller includes a termination resistor in packaging of its die.

15. (Original) The system of claim 11, wherein at least two of the integrated circuits include a termination resistor in its die.

16. (Original) The system of claim 11, wherein at least one of the integrated circuits includes a termination resistor in packaging of its die.

17. (Original) The system of claim 11, wherein one of the integrated circuits acts as a master controller for the other integrated circuits.

18. (Original) The system of claim 11, wherein the integrated circuits use differential signaling.

19. (Original) The system of claim 11, wherein the integrated circuits use pseudo differential signaling.

20. (Original) A system comprising:

a group of integrated circuits connected in a pseudo differential arrangement in which multiple conductors carrying signals share a common reference signal conductor.

21. (Original) The system of claim 20, wherein the integrated circuits are part of a multidimensional ring.

22. (Original) The system of claim 21, wherein the ring includes truncated ring portions.

23. (Original) The system of claim 20, wherein some of the signal carrying conductors have one reference signal conductor and others of the signal carrying conductors have another reference signal conductor.

24. (Original) The system of claim 20, wherein at least one of the integrated circuits that is not a master controller includes a termination resistor in its die.

25. (Original) The system of claim 20, wherein at least one of the integrated circuits that is not a master controller includes a termination resistor in packaging of its die.

26. (Original) The system of claim 20, wherein at least two of the integrated circuits

include a termination resistor in its die.

27. (Original) The system of claim 20, wherein at least one of the integrated circuits includes a termination resistor in packaging of its die.

28. (Original) The system of claim 20, wherein one of the integrated circuits acts as a master controller for the other integrated circuits.